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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 3

Complete if Known	
Application Number	10/065,340
Filing Date	10/06/2002
First Named Inventor	MELVIN
Art Unit	2186
Examiner Name	S. Elmore
Attorney Docket Number	

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] -Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature	S. Elmore	Date Considered	1-25-2005

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 2 of 3

Complete if Known	
Application Number	10/065,340
Filing Date	10/06/2002
First Named Inventor	HELVIN
Group Art Unit	2186
Examiner Name	Elmore
Attorney Docket Number	

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
		SEE ATTACHED SHEET	

Examiner Signature	S. Elmore	Date Considered	1-25-2005

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT – Page 3 of 3
Application Number: 10/065,340
Filing Date: 10/06/2002
Applicant: Stephen Waller Melvin

Cite	Non Patent Publication
1	S. MELVIN and Y. PATT, "Handling of Packet Dependencies: A Critical Issue for Highly Parallel Network Processors," *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems*, October 8-11, 2002, Grenoble, France
2	M. FRANKLIN AND G. SOHI, "ARB: *A hardware mechanism for dynamic reordering of memory references," IEEE* Transactions on Computers, vol. 45, pp. 552-571, May 1996.
3	S. GOPAL, T. N. VIJAKUMAR, J. E. SMITH AND G. S. SOHI, "Speculative versioning cache," *Proceedings of the Fourth International Symposium on High-Performance Computer Architecture*, Las Vegas, February 1998.
4	G. SOHI, S. BREACH, AND T. VIJAYKUMAR, "Multiscalar processors," *Proceedings of the 22nd Annual International Symposium on Computer Architecture*, pp. 414-425, Ligure, Italy, June 1995.
5	J. G. STEFFAN AND T. MOWRY, "The potential for using thread-level data speculation to facilitate automatic parallelization," *Proceedings of the Fourth International Symposium on High-Performance Computer Architecture*, Las Vegas, February, 1998.
6	L. HAMMOND, M. WILLEY, AND KUNLE OLUKOTUN, "Data Speculation Support for a Chip Multiprocessor," *Proceedings of the Eighth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-VIII)*, San Jose, October 1998.
7	J. STEFFAN, C. COLOHAN, ANTONIA ZHAI, AND T. MOWRY, "A Scalable Approach to Thread-Level Speculation," *Proceedings of the 27th Annual International Symposium on Computer Architecture*, Vancouver, Canada, June 2000.
8	M. CINTRA, J. MARTINEZ, AND J. TORRELLAS, "Architectural Support for Scalable Speculative Parallelization in Shared-Memory Multiprocessors," *Proceedings of the 27th Annual International Symposium on Computer Architecture*, Vancouver, Canada, June 2000.
9	J. MARTINEZ AND J. TORRELLAS, "Speculative Locks for Concurrent Execution of Critical Sections in Shared-Memory Multiprocessors," *Workshop on Memory Performance Issues, International Symposium on Computer Architecture*, Göteborg, Sweden , June, 2001.
10	R. RAJWAR AND J. GOODMAN, "Speculative Lock Elision: Enabling Highly Concurrent Multithreaded Execution," *Proceedings of the 34th Annual International Symposiumon Microarchitecture*, Austin, Texas, December 2001.
11	M. HERLIHY AND J. E. B. MOSS, "Transactional Memory: Architectural support for lock-free data structures," *Proceeedings of the International Conference on Computer Architecture*, pp. 289-300, San Diego, California, May 1993.